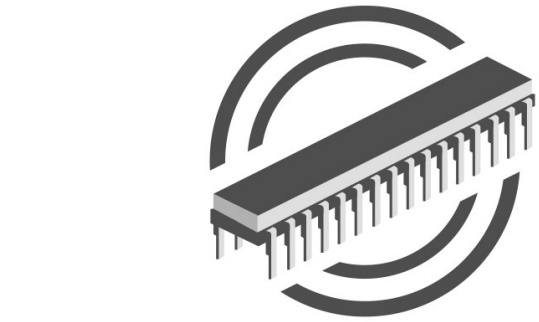

Retrotroniks

RetroCPLD

Compiler User Manual

Logic design, fitting, JEDEC generation, and device reference

Edition 1 • September 2026

Command-line edition for macOS, Windows, and Linux

About this manual

This manual describes the implemented RetroCPLD language and command-line workflow. It is a practical reference, not a claim of complete CUPL compatibility. Device names, package choices, electrical limits, and programming procedures must match the actual part and board.

> **Safety policy** RetroCPLD deliberately keeps the ATF15xx JTAG pins reserved. They cannot be assigned as ordinary I/O. This preserves the normal programming and recovery path.

Contents

Part	What it covers
1. Getting started	Install, compile, output files, errors, and licensing
2. Language reference	Declarations, equations, nodes, clocks, controls, configuration, comments, and signatures
3. Device guides	ATF1502, ATF1504, GAL16V8, GAL20V8, and GAL22V10
4. Editor integration	Terminal, VS Code, Xcode, and other editors/build systems
5. Design practice	Electrical cautions, verification, diagnostics, and compatibility notes
Appendices	Quick syntax, examples, package functions, and current limitations

Product editions

Mode	Enabled targets
LIMITED	ATF1502AS, ATF1502ASV, GAL20V8B
FULL	All LIMITED targets plus ATF1504AS, ATF1504ASV, GAL16V8B, GAL22V10B

A license is portable and is not locked to one computer. RetroCPLD performs license verification locally; normal compilation does not require an online check.

1. Getting started

What RetroCPLD does

- Reads a compact equation-based source file, validates it for the selected device and package, fits the design, and writes a JEDEC (.jed) fuse file.
- Supports combinational equations, registered outputs, internal nodes, product-term output enable, supported clock/reset/preset controls, signatures, and device-specific configuration.
- Rejects illegal pins, unsupported feature combinations, routing conflicts, and resource overflow before producing a new output file.

What it does not do

- It does not program a device. Use a programming method compatible with your part and generated JEDEC.
- It does not perform board-level electrical or timing verification.
- It is not a drop-in compiler for arbitrary WinCUPL source. FIELD/bus declarations, state-machine statements, libraries, CUPL headers, and .D/.CK notation are not implemented.
- It does not repurpose ATF JTAG pins as user I/O.

Install the command

Place the rcpld executable in a folder on your command search path, or invoke it with its full path. On macOS/Linux, ensure the executable bit is set. On Windows, use rcpld.exe. No IDE is required.

```
rcpld design.rcpld
```

A successful compile creates design.jed beside design.rcpld. A failed compile returns a nonzero status and must not replace a previously existing JEDEC. Always read the final compiler result before using an output file.

Minimal source

```
DEVICE ATF1502AS
PACKAGE PLCC44
PIN 2 SWITCH INPUT
PIN 4 LED OUTPUT
LED = SWITCH
```

Source files are plain text. The .rcpld extension is recommended but the compiler accepts a source filename supplied on the command line.

Registration

```
rcpld --license-status
rcpld --install-license /path/to/retrocpld.license
rcpld --license /path/to/retrocpld.license design.rcpld
```

- --license-status reports LIMITED or FULL operation and the recognized license.
- --install-license validates and copies a license into the normal per-user location.
- --license uses a portable license for that invocation without installing it.
- RETROCPLD_LICENSE_FILE may point to a license for IDE or build-system integration.

- A file named retrocpld.license beside the executable is also recognized.

Platform	Installed license location
macOS / Linux	~/.retrocpld/license.lic
Windows	%APPDATA%\RetroCPLD\license.lic

2. Source-file structure

A source normally follows this order: DEVICE, optional PACKAGE or GAL_MODE, optional SIGNATURE/POWER_DOWN/CONFIG declarations, PIN and NODE declarations, then equations. Semicolons are optional separators; newlines are whitespace, not statement terminators.

```
DEVICE ATF1504ASV
PACKAGE TQFP100
SIGNATURE = 0x1234

PIN 87 CLOCK INPUT GCLK1
PIN 8 ENABLE INPUT
PIN 10 Q OUTPUT REGISTERED GCLK1 CE PRODUCT

Q = !Q
Q.CE = ENABLE
```

Names and keywords

- Keywords and signal names are case-sensitive.
- A name may contain letters, digits, and underscores, but cannot begin with a digit.
- Do not reuse reserved keywords or directive names as signals.
- Every declared output and NODE needs exactly one ordinary equation. Required control equations are additional assignments.

Comments

```
// line comment
LED = SWITCH   // comment after an equation

/* block comments may
  span lines */
```

Block comments do not nest. An unterminated block comment is an error. The exclamation mark remains logical NOT; it does not begin a comment.

Numbers

Boolean constants are 0 and 1. Signature values may be written in hexadecimal (0x), decimal, or leading-zero octal; hexadecimal is strongly recommended because its width is obvious.

Boolean expressions

Operator	Meaning	Precedence
!	NOT	highest
&	AND	2
^	XOR	3
|	OR	lowest

```
MATCH = ENABLE & (A ^ B)
ACTIVE_LOW = !SWITCH
ANY = A | B | C
```

Parentheses make intent explicit. The fitter converts expressions to the target architecture and reports when product terms, routing, or device-specific constraints cannot be satisfied.

3. Declarations and equations

Device and package

```
DEVICE ATF1504AS
PACKAGE PLCC84
```

DEVICE	Packages	Default
ATF1502AS / ATF1502ASV	PLCC44, TQFP44	PLCC44
ATF1504AS / ATF1504ASV	PLCC44, TQFP44, PLCC84, TQFP100	PLCC84
GAL16V8B	DIP20	DIP20
GAL20V8B	DIP24	DIP24
GAL22V10B	DIP24	DIP24

Voltage AS and ASV names use the same architecture and logic fuse map. AS parts are 5 V devices; ASV parts are 3.3 V devices. RetroCPLD cannot enforce the voltage used on your board. Select the name printed on the part and wire it within its datasheet limits.

Pins

```
PIN number name INPUT [GCLK1|GCLK2|GCLK3] [GCLR] [GOE1|GOE2|GOE6]
PIN number name OUTPUT [REGISTERED] [GCLK1|GCLK2|GCLK3]
   [OE ALWAYS|OE1|OE2|GOE6|PRODUCT]
   [RESET GCLR|PRODUCT] [CE PRODUCT] [PRESET PRODUCT]
```

Modifiers must appear in the shown order. Availability depends on the target. Physical power, ground, and JTAG pins are rejected as ordinary signals. Package-specific dedicated functions must be declared on their correct physical pins.

Ordinary equations

```
SUM = A ^ B
DECODE = !A15 & A14 & A13
LED = DECODE | FORCE_LED
```

A registered output equation describes the next value presented to its D input. Referring to the registered output name reads its current feedback state.

```
PIN 43 CLOCK INPUT GCLK1
PIN 12 Q OUTPUT REGISTERED GCLK1
Q = !Q
```

Clock required This divider toggles only on valid external clock edges. It does not blink by itself. Use a common electrical ground between the clock source and target board, and keep unused inputs at defined levels.

Control equations

```
PIN 4 Q OUTPUT REGISTERED GCLK1 OE PRODUCT RESET PRODUCT CE PRODUCT
Q = DATA
Q.OE = OUTPUT_ENABLE
Q.RESET = CLEAR_REQUEST
Q.CE = COUNT_ENABLE

PIN 5 R OUTPUT REGISTERED GCLK1 PRESET PRODUCT
R = DATA
R.PRESET = SET_REQUEST
```

Control	Meaning	Requirement
.OE	Active-high product-term output enable	OUTPUT ... OE PRODUCT
.RESET	Active-high local asynchronous reset	OUTPUT/NODE ... RESET PRODUCT
.CE	Clock enable with GCLK; local clock when no GCLK is selected	... CE PRODUCT
.PRESET	Active-high asynchronous preset	... PRESET PRODUCT

Each product control must reduce to exactly one product term. These controls consume dedicated macrocell terms and can reduce room for data logic or conflict with cascade. The fitter checks the combination.

4. Internal nodes and registered resources

```
NODE DECODE
DECODE = A & B

NODE STATE REGISTERED GCLK1
STATE = !STATE
```

On ATF devices, NODEs consume internal macrocells and routing resources. A buried registered NODE keeps its package output driver disabled. Registered NODEs support the same applicable reset, clock-enable, preset, low-power, storage, and toggle configuration as registered physical outputs.

On GAL devices, NODEs are combinational aliases expanded into consuming equations. They must be acyclic. Registered NODE declarations are rejected.

Global clock and clear

```
PIN 43 CLOCK INPUT GCLK1
PIN 1 CLEAR_N INPUT GCLR
PIN 12 Q OUTPUT REGISTERED GCLK1 RESET GCLR
Q = DATA
```

GCLR is an asynchronous global clear path. The signal name may suggest active-low or active-high board logic, but the physical global function and optional CONFIG inversion determine behavior. Do not assume the signal name changes polarity.

Local product-term clock

```
PIN 8 LOCAL_CLOCK INPUT
PIN 4 Q OUTPUT REGISTERED CE PRODUCT
Q = !Q
Q.CE = LOCAL_CLOCK
```

When CE PRODUCT is used without GCLK1/GCLK2/GCLK3, .CE becomes the PT4 local clock. With a global clock selected, .CE is a clock enable. Avoid combinational glitches on any clock equation.

Native XOR and toggle register

```
PIN 12 Q OUTPUT REGISTERED GCLK1
Q = ENABLE
CONFIG Q XOR TOGGLE
```

In toggle mode, Q = 0 holds state and Q = 1 toggles on each selected clock edge. A product term may be the toggle condition. Toggle mode requires DFF storage and cannot be combined with a ^ data equation or FAST_INPUT.

A top-level A ^ B can use the ATF macrocell XOR path when one side fits a single product term. More complex XOR expressions preserve Boolean meaning through ordinary sum-of-products expansion when the selected device allows it.

5. ATF configuration reference

CONFIG uses three space-separated fields and no equals sign:

```
CONFIG target option value
```

Target	Option	Accepted values
DEVICE	TERMINATION	BUS_KEEPER, HIGH_Z
DEVICE	RESET_HYSTERESIS	LARGE, SMALL

Target	Option	Accepted values
DEVICE	READ_PROTECTION	ON, OFF
CLK1 / CLK2 / CLK3	STANDBY_WAKEUP	ON, OFF
TMS / TDI	TERMINATION	PULL_UP, HIGH_Z
GCLK1 / GCLK2 / GCLK3 / GCLR	INVERT	ON, OFF
output	SLEW	FAST, SLOW
output	DRIVER	OPEN_DRAIN, PUSH_PULL
output or NODE	LOW_POWER	ON, OFF
registered output or NODE	STORAGE	DFF, LATCH
GOE1 … GOE6	SOURCE	declared signal name
GOE1 … GOE6	INVERT	ON, OFF
output	GLOBAL_OE	GOE1 … GOE6
registered NODE	FAST_INPUT	ordinary INPUT signal
registered output or NODE	XOR	TOGGLE

Omitted options preserve the compiler baseline for that device. Duplicate target/option pairs, unknown values, wrong consumer types, and impossible routes are errors.

Important configuration behavior

- OPEN_DRAIN requires an external pull-up and cannot actively drive high.
- LOW_POWER can reduce speed. SLEW affects an output driver, not the logic equation.
- STORAGE LATCH selects level-sensitive storage rather than an edge-triggered D flip-flop.
- Global clock inversion affects every registered consumer of that global clock.
- STANDBY_WAKEUP fuses exist in the map, but operational standby wakeup is associated with low-power variants and is not promised for ordinary AS parts.
- READ_PROTECTION changes device security information. Leave it OFF during development and confirm the final programming flow before enabling it.

ATF1502 GOE inversion exception

Known limitation CONFIG GOEn INVERT ON is rejected for ATF1502. The polarity fuse programmed and verified during testing but did not invert the tested route. Obtain the opposite logic polarity in the source equation instead, for example ENABLE_ROUTE = !ENABLE. ATF1504 internal GOE inversion is supported.

Internal global output enable

```
CONFIG GOE3 SOURCE ENABLE_FB
CONFIG GOE3 INVERT OFF
CONFIG LED GLOBAL_OE GOE3
```

SOURCE must be declared and physically routable. A pad INPUT uses its pad route; an OUTPUT or NODE uses macrocell feedback. Every configured source needs at least one consumer, and every consumer needs a source. Internal GOE cannot overwrite an incompatible package OE route.

6. Signature and power-down

User signature

```
SIGNATURE = 0x1234                  // ATF: 16 bits
SIGNATURE = 0x0 123 456 789ABCDEF      // GAL: 64 bits
```

The user signature is application metadata stored in device fuses. It is unrelated to RetroCPLD registration or code protection. ATF signatures are 16 bits. GAL signatures are 64 bits. If omitted, the current defaults are ATF1502 0xFFFF, ATF1504 0x0000, and GAL zero.

Power-down

```
POWER_DOWN PD1
POWER_DOWN PD2
```

Package	PD1	PD2
ATF1502 PLCC44	11	25
ATF1502 TQFP44	5	19
ATF1504 PLCC44	11	25
ATF1504 TQFP44	5	19
ATF1504 PLCC84	20	46
ATF1504 TQFP100	12	42

POWER_DOWN is opt-in. The selected pin becomes a power-down input and cannot also be declared as ordinary I/O. Never leave an enabled power-down input floating. GAL targets reject POWER_DOWN.

Direct-pad input register

```
PIN 83 CLOCK INPUT GCLK1
PIN 35 DATA INPUT
NODE CAPTURE REGISTERED GCLK1
CAPTURE = DATA
CONFIG CAPTURE FAST_INPUT DATA
```

FAST_INPUT binds the registered NODE to DATA's macrocell and bypasses the AND array. The equation must be exactly CAPTURE = DATA; negation and additional logic are rejected. DATA must be an ordinary non-JTAG macrocell input, not a dedicated clock pad.

7. ATF1502AS and ATF1502ASV

The ATF1502 family provides 32 macrocells in two logic array blocks. RetroCPLD supports PLCC44 and TQFP44; PLCC44 is the default. AS and ASV use the same compiler architecture. Choose the exact DEVICE name for the part marking and observe its supply voltage.

Function	PLCC44	TQFP44
GCLK1	43	37
GCLK2 / OE2	2	40
GCLK3	41	35
GCLR	1	39
OE1	44	38
PD1 / PD2	11 / 25	5 / 19
TDI / TMS	7 / 13	1 / 7
TCK / TDO	32 / 38	26 / 32
Ground	10, 22, 30, 42	4, 16, 24, 36
VCC	3, 15, 23, 35	9, 17, 29, 41

Supported design features

- Combinational and registered outputs, feedback, and buried nodes.
- GCLK1/GCLK2/GCLK3, local PT4 clock, global GCLR, clock enable, product reset, product preset, package OE, product OE, and internal GOE routing.
- Native PT2 XOR and toggle-register mode, user signature, power-down selection, output driver/slew, low-power and latch configuration.
- Automatic device-specific fitting and JEDEC generation while retaining JTAG reservations.

ATF1502 example: registered toggle with enable

```
DEVICE ATF1502AS
PACKAGE PLCC44
PIN 43 CLOCK INPUT GCLK1
PIN 2 ENABLE INPUT
PIN 4 Q OUTPUT REGISTERED GCLK1 CE PRODUCT
Q = !Q
Q.CE = ENABLE
```

8. ATF1504AS and ATF1504ASV

The ATF1504 family provides 64 macrocells in four logic array blocks. RetroCPLD supports PLCC44, TQFP44, PLCC84, and TQFP100; PLCC84 is the default. Package selection changes physical lead bonding, not the 64-macrocell fuse architecture. Unbonded macrocells remain usable as internal logic resources.

Function	PLCC44	TQFP44	PLCC84	TQFP100
GCLK1	43	37	83	87
GCLK2 / OE2	2	40	2	90
GCLK3	41	35	81	85
GCLR	1	39	1	89
OE1	44	38	84	88
PD1 / PD2	11 / 25	5 / 19	20 / 46	12 / 42
TDI / TMS	7 / 13	1 / 7	14 / 23	4 / 15
TCK / TDO	32 / 38	26 / 32	62 / 71	62 / 73

Power and ground pins

Package	Ground	Core VCC	I/O VCC
PLCC44	10, 22, 30, 42	3, 15, 23, 35	same supply domain
TQFP44	4, 16, 24, 36	9, 17, 29, 41	same supply domain
PLCC84	7, 19, 32, 42, 47, 59, 72, 82	3, 43	13, 26, 38, 53, 66, 78
TQFP100	11, 26, 38, 43, 59, 74, 86, 95	39, 91	3, 18, 34, 51, 66, 82

ATF1504 supports the ATF features described earlier, plus automatic cascade expansion when an equation exceeds a macrocell's native data-term capacity. Cascade uses neighboring macrocells and is subject to chain boundaries, occupied suppliers, and control-term conflicts. A fit success means the requested route was found; it is not timing analysis.

PLCC84 example

```
DEVICE ATF1504AS
PACKAGE PLCC84
PIN 83 CLOCK INPUT GCLK1
PIN 35 ENABLE INPUT
PIN 60 Q OUTPUT REGISTERED GCLK1 CE PRODUCT
Q = !Q
Q.CE = ENABLE
```

JTAG safety

Reserved pins TDI, TMS, TCK, and TDO remain dedicated JTAG pins in every supported ATF package. RetroCPLD does not provide syntax to reclaim them as user I/O.

9. GAL device guides

GAL16V8B and GAL20V8B

These parts use an architecture-specific fitter with SIMPLE, COMPLEX, and REGISTERED policies. GAL_MODE may select a policy explicitly or allow AUTO fitting.

```
GAL_MODE = AUTO
GAL_MODE = SIMPLE
GAL_MODE = COMPLEX
GAL_MODE = REGISTERED
```

Target	Package	Clock	Shared OE	Status
GAL16V8B	DIP20	pin 1, GCLK1	pin 11, GOE1	Software-verified; hardware validation pending
GAL20V8B	DIP24	pin 1, GCLK1	pin 13, GOE1	Hardware-validated representative modes

A registered GAL16V8B or GAL20V8B output must declare GCLK1 and OE OE1. The design must declare the dedicated clock and GOE input pins. Any registered output selects registered mode for the entire device. Combinational outputs may coexist subject to that mode's pin and product-term rules.

```
DEVICE GAL20V8B
GAL_MODE = REGISTERED
PIN 1 CLOCK INPUT GCLK1
PIN 13 ENABLE_N INPUT GOE1
PIN 22 Q OUTPUT REGISTERED GCLK1 OE OE1
Q = !Q
```

In SIMPLE mode, an output may use eight data product terms but has restricted feedback/input behavior. COMPLEX mode provides programmable product OE and its mode-specific feedback routes. AUTO tries legal

modes for a combinational design. Let the fitter report actual capacity and pin restrictions rather than assuming modes are interchangeable.

GAL22V10B

GAL22V10B uses DIP24 and ten individually configured output macrocells on pins 14 through 23. It does not use GAL_MODE. Registered outputs use pin 1 as GCLK1. Outputs support ALWAYS or PRODUCT output enable, with device-specific product-term capacities.

```
DEVICE GAL22V10B
PIN 1 CLOCK INPUT GCLK1
PIN 2 DATA INPUT
PIN 23 Q OUTPUT REGISTERED GCLK1
Q = DATA
```

Current GAL22V10 limitation The architecture's global asynchronous-reset and synchronous-preset rows are not yet exposed. RESET, CE, and PRESET syntax is rejected for GAL22V10B instead of being mapped incorrectly from ATF per-output controls. Hardware validation is pending.

All GAL targets support combinational NODE aliases and a 64-bit SIGNATURE. ATF CONFIG, POWER_DOWN, GCLR, CE, PRESET, and ATF-style internal GOE routing are not GAL features.

10. Editor and build integration

Any editor that can save plain text and run a command can use RetroCPLD. The compiler remains a command-line tool so projects are portable and scripts can reproduce builds.

VS Code

Create a .vscode/tasks.json file in the project folder. This example compiles the currently open file and reports compiler messages in the terminal:

```
{
  "version": "2.0.0",
  "tasks": [{
    "label": "Compile RetroCPLD",
    "type": "shell",
    "command": "rcpld",
    "args": ["${file}"],
    "group": { "kind": "build", "isDefault": true },
    "problemMatcher": []
  }]
}
```

Use Run Build Task to invoke it. If rcpld is not on PATH, replace command with the full executable path. A future language extension may add syntax coloring, but compilation does not depend on one.

Xcode

Add a Run Script build phase or an External Build System target whose command invokes rcpld with the design file. Quote paths containing spaces. Keep generated .jed files in a predictable output folder or beside the source.

```
"/full/path/to/rcpld" "/full/path/to/design.rcpld"
```

Other editors and make

```
design.jed: design.rcpld
	rcpld design.rcpld
```

The same pattern works in shell scripts, Make, Ninja, CI systems, and editor task runners. Check the process exit code. Never continue to a programming step after a failed compilation merely because an older .jed file exists.

Portable license in builds

```
RETROCPLD_LICENSE_FILE=/secure/path/retrocpld.license rcpld design.rcpld
```

Keep customer licenses out of public repositories and shared build logs.

11. Electrical and verification practice

RetroCPLD verifies logic legality and fuse encoding; the hardware designer remains responsible for supply voltage, pinout, signal levels, loading, timing, and programming compatibility.

- Use every required device power and ground pin and place appropriate decoupling close to the package.
- Give external clock sources and the target board a common ground reference.
- Do not leave clocks, reset, power-down, output-enable, or ordinary CMOS inputs floating. Use a suitable pull resistor when the driving source can disconnect or become high impedance.
- An OPEN_DRAIN output needs an external pull-up sized for the voltage, current, and speed required.
- A logic-low output can sink current—such as the return current for a properly limited LED—within the device output rating. It is still an active I/O driver, not a substitute for the board's power ground or a signal-generator reference.
- A logic-high output is not a 5 V or 3.3 V supply rail. Do not use it to power external circuitry.
- Check the selected package before wiring. The same macrocell can appear on a different physical pin or be unbonded in another package.
- Treat a successful fit as a prerequisite, not proof that timing or electrical margins are met.

Recommended workflow

Step	Action
1	Select the exact DEVICE and PACKAGE.
2	Compile and resolve every diagnostic.
3	Confirm the reported package and inspect the output timestamp/name.
4	Program with a compatible method and verify the write.
5	Power the circuit within the part rating and test simple I/O first.
6	Add clocks, enables, registered behavior, and complex routing incrementally.

Step	Action
7	Keep a known-good source and JEDEC for regression testing.

Read protection

Keep READ_PROTECTION OFF while developing and debugging. Enable it only for a deliberate release image after confirming your programming and recovery procedure. Security behavior can affect readback and final programming sequence.

12. Diagnostics and compatibility

Common compiler errors

Message category	What to check
Unknown/unsupported device	Use an exact supported DEVICE name; registration may be required.
Invalid package or pin	Select the matching PACKAGE and use a legal physical I/O or dedicated-function pin.
Missing equation	Every OUTPUT and NODE needs one ordinary equation.
Undefined signal	Declare the input/output/node and check capitalization.
Product-term overflow	Simplify logic, move logic into NODEs, or free conflicting control/cascade resources.
No route / placement conflict	A requested pad, feedback tap, FAST_INPUT, GOE, or cascade resource cannot coexist with current placement.
Missing control equation	OE PRODUCT, RESET PRODUCT, CE PRODUCT, or PRESET PRODUCT requires its matching dotted equation.
License error	Check --license-status, install the signed file, or select a LIMITED-mode target.

Differences from WinCUPL

Area	RetroCPLD behavior
File header	Uses DEVICE directly; CUPL Name/PartNo/Revision/Designer/Company/Assembly/Location headers are not implemented.
Pins	Uses PIN number name INPUT/OUTPUT with explicit register/control modifiers.

Area	RetroCPLD behavior
Equations	Uses = with !, &, ^, | and parentheses; semicolons are optional.
Registered logic	Declare OUTPUT REGISTERED and write its next-state equation; .D and .CK notation are not supported.
Buses / FIELD	Not implemented; declare individual signals.
State machines	No state-machine statements. Build state registers and next-state/output equations explicitly.
Libraries/macros	Not implemented.
Device configuration	Uses RetroCPLD CONFIG declarations rather than CUPL device-property syntax.
Comments	Supports // and /* ... */.
Output	Writes a JEDEC beside the source after a successful fit.

State machines with equations

Although dedicated state-machine syntax is not implemented, registered equations can describe state. Declare one or more registered outputs or NODEs, refer to their feedback names, and write each next-state equation. Keep the design small enough for available product terms and test reset behavior explicitly.

```
DEVICE ATF1502AS
PACKAGE PLCC44
PIN 43 CLOCK INPUT GCLK1
PIN 1 CLEAR INPUT GCLR
NODE S0 REGISTERED GCLK1 RESET GCLR
NODE S1 REGISTERED GCLK1 RESET GCLR
S0 = !S0
S1 = S1 ^ S0
```

Appendix A — Quick syntax sheet

```
DEVICE device_name
PACKAGE PLCC44|TQFP44|PLCC84|TQFP100
GAL_MODE = AUTO|SIMPLE|COMPLEX|REGISTERED
SIGNATURE = number
POWER_DOWN PD1
POWER_DOWN PD2

PIN number name INPUT [GCLK1|GCLK2|GCLK3] [GCLR] [GOE1|GOE2|GOE6]
PIN number name OUTPUT [REGISTERED] [GCLK1|GCLK2|GCLK3]
   [OE ALWAYS|OE1|OE2|GOE6|PRODUCT]
   [RESET GCLR|PRODUCT] [CE PRODUCT] [PRESET PRODUCT]

NODE name
NODE name REGISTERED GCLK1|GCLK2|GCLK3
   [RESET GCLR|PRODUCT] [CE PRODUCT] [PRESET PRODUCT]

name = expression
name.OE = product_expression
name.RESET = product_expression
name.CE = product_expression
name.PRESET = product_expression

CONFIG target option value
```

Operators

Syntax	Meaning
!A	NOT
A & B	AND
A ^ B	XOR
A | B	OR
(expression)	grouping
0 / 1	Boolean constants

Supported device names

```
ATF1502AS   ATF1502ASV
ATF1504AS   ATF1504ASV
GAL16V8B    GAL20V8B    GAL22V10B
```

Appendix B — Complete examples

Combinational decode

```
DEVICE ATF1502AS
PACKAGE PLCC44
PIN 2 A INPUT
PIN 4 B INPUT
PIN 5 ENABLE INPUT
PIN 6 Y OUTPUT
Y = ENABLE & (A ^ B)
```

Registered divide-by-two with asynchronous clear

```
DEVICE ATF1504AS
PACKAGE PLCC84
PIN 83 CLOCK INPUT GCLK1
PIN 1 CLEAR INPUT GCLR
PIN 60 Q OUTPUT REGISTERED GCLK1 RESET GCLR
Q = !Q
```

Tri-state output with product enable

```
DEVICE GAL20V8B
GAL_MODE = COMPLEX
PIN 2 DATA INPUT
PIN 3 ENABLE INPUT
PIN 22 BUS_OUT OUTPUT OE PRODUCT
BUS_OUT = DATA
BUS_OUT.OE = ENABLE
```

Internal GOE on ATF1504

```
DEVICE ATF1504AS
PACKAGE PLCC84
PIN 35 ENABLE INPUT
PIN 36 DATA INPUT
PIN 60 BUS_OUT OUTPUT
NODE ENABLE_ROUTE
ENABLE_ROUTE = ENABLE
BUS_OUT = DATA
CONFIG GOE3 SOURCE ENABLE_ROUTE
CONFIG GOE3 INVERT OFF
CONFIG BUS_OUT GLOBAL_OE GOE3
```

Open-drain output

```
DEVICE ATF1502AS
PACKAGE PLCC44
PIN 2 ASSERT INPUT
PIN 4 IRQ OUTPUT
IRQ = ASSERT
CONFIG IRQ DRIVER OPEN_DRAIN
```

Appendix C — Current qualification notes

RetroCPLD's ATF1502AS and ATF1504AS core paths and representative configuration features have been exercised on hardware, including combinational I/O, registered logic, clocks, enables, reset/preset behavior, internal routing, native XOR/toggle behavior, signatures, power-down, and ATF1504 cascade. ASV targets share their corresponding AS fuse architecture; users must still validate voltage-specific hardware behavior.

GAL20V8B representative SIMPLE, COMPLEX, and REGISTERED designs have been exercised on hardware. GAL16V8B and GAL22V10B have device-specific software models and regression coverage; physical-device validation remains pending. Their inclusion should not be read as a timing or electrical guarantee.

Timing characterization—including propagation delay, setup/hold margin, and slew-rate measurement—requires suitable test equipment and remains the responsibility of the design and device qualification process.

Versioning and support

Keep the compiler version, source file, selected package, generated JEDEC, and programming result together when reporting a problem. Include the complete compiler diagnostic and a minimal source file when possible. Do not send a private license file or any seller signing key.

> **Documentation scope** This edition documents the implemented compiler as of September 2026. Later builds may add targets or syntax; use the manual supplied with the installed version.

Appendix D — Syntax reference lookup

Use this alphabetical lookup when writing or checking a source file. Brackets show optional fields. A vertical bar separates alternatives; do not type the brackets or vertical bars.

Directives declarations and equations

Entry	Exact form	Use and restrictions
CE equation	name.CE = product_expression	Required by CE PRODUCT. With a selected GCLK it is an active-high clock enable; without a GCLK on an ATF output it is the PT4 local clock.
CONFIG	CONFIG target option value	Sets an ATF device, global, macrocell, or special-pin option. Do not use an equals sign.
DEVICE	DEVICE device_name	Required target selection. Accepted names: ATF1502AS, ATF1502ASV, ATF1504AS, ATF1504ASV, GAL16V8B, GAL20V8B, GAL22V10B.
GAL_MODE	GAL_MODE = AUTO|SIMPLE|COMPLEX|REGISTERED	Optional fitting policy for GAL16V8B and GAL20V8B only. GAL22V10B does not use GAL_MODE.
NODE combinational	NODE name	Declares an internal ATF macrocell or an acyclic GAL combinational alias. Follow it with name = expression.
NODE registered	NODE name REGISTERED GCLK1|GCLK2|GCLK3 [RESET GCLR|PRODUCT] [CE PRODUCT] [PRESET PRODUCT]	Declares a buried ATF register. A matching physical clock input is required. Registered GAL NODEs are not supported.
OE equation	name.OE = product_expression	Required by OE PRODUCT. The expression is an active-high output-enable term.
PACKAGE	PACKAGE PLCC44|TQFP44|PLCC84|TQFP100	ATF package selection. ATF1502 accepts PLCC44 or TQFP44. ATF1504 accepts all four. Omit only when the documented default is intended.
PIN input	PIN number name INPUT [GCLK1|GCLK2|GCLK3] [GCLR] [GOE1|GOE2|GOE6]	Declares a physical input and, when present, its dedicated clock, clear, or package output-enable function. The selected device and package determine legality.

Entry	Exact form	Use and restrictions
PIN output	PIN number name OUTPUT [REGISTERED] [GCLK1|GCLK2|GCLK3] [OE ALWAYS|OE1|OE2|GOE6|PRODUCT] [RESET GCLR|PRODUCT] [CE PRODUCT] [PRESET PRODUCT]	Declares a physical output. Modifiers must appear in this order and must be supported by the selected target.
POWER_DOWN	POWER_DOWN PD1 or POWER_DOWN PD2	Reserves the selected ATF power-down pin. The pin cannot also be ordinary I/O and must not float. GAL targets reject this directive.
PRESET equation	name.PRESET = product_expression	Required by PRESET PRODUCT. It is an active-high asynchronous preset term.
RESET equation	name.RESET = product_expression	Required by RESET PRODUCT. It is an active-high local asynchronous-reset term.
SIGNATURE	SIGNATURE = number	Stores a 16-bit ATF or 64-bit GAL user signature. Hexadecimal form is recommended.
Signal equation	name = expression	Defines an OUTPUT or NODE. A registered target equation specifies its next state; reading that name in another expression uses feedback.

Pin and register modifiers

Modifier	Meaning	Important condition
CE PRODUCT	Product-term clock enable or local clock	Requires name.CE. With no GCLK it becomes an ATF local clock.
GCLK1 / GCLK2 / GCLK3	Selects a global clock path	Declare the matching physical clock INPUT. Device and package pin assignments differ.
GCLR	Selects or declares global asynchronous clear	A registered consumer using RESET GCLR needs a matching physical INPUT GCLR declaration.
GOE1 / GOE2 / GOE6	Declares a package global output-enable input	Only the package-supported function and physical pin are legal.
OE ALWAYS	Keeps the output driver enabled	Default for ordinary combinational and supported registered outputs.
OE OE1 / OE2 / GOE6	Selects a package output-enable path	Declare its matching package OE input. Polarity is device-specific.

Modifier	Meaning	Important condition
OE PRODUCT	Selects product-term output enable	Requires name.OE. It cannot share PT5 with PRESET PRODUCT on the same ATF macrocell.
PRESET PRODUCT	Selects product-term asynchronous preset	Requires name.PRESET and a registered target. It cannot share PT5 with OE PRODUCT.
REGISTERED	Uses the target macrocell register	Requires a global clock or the supported ATF local-clock form.
RESET GCLR	Selects global asynchronous clear	Requires a matching INPUT GCLR declaration.
RESET PRODUCT	Selects local product-term asynchronous reset	Requires name.RESET and exactly one product term.

CONFIG options

Target and option	Values	Purpose
DEVICE TERMINATION	BUS_KEEPER, HIGH_Z	Selects the ATF device-wide input termination baseline.
DEVICE RESET_HYSTERESIS	LARGE, SMALL	Selects reset hysteresis.
DEVICE READ_PROTECTION	ON, OFF	Controls read protection. Leave OFF during normal development.
CLK1|CLK2|CLK3 STANDBY_WAKEUP	ON, OFF	Controls the mapped standby-wakeup fuse.
TMS|TDI TERMINATION	PULL_UP, HIGH_Z	Selects termination for the dedicated JTAG input.
GCLK1|GCLK2|GCLK3|GCLR INVERT	ON, OFF	Inverts the selected used global function for all of its consumers.
output SLEW	FAST, SLOW	Selects output slew rate.
output DRIVER	OPEN_DRAIN, PUSH_PULL	Selects the output driver. OPEN_DRAIN requires an external pull-up.
output|NODE LOW_POWER	ON, OFF	Selects the mapped low-power macrocell option.
registered output|NODE STORAGE	DFF, LATCH	Selects edge-triggered or level-sensitive storage.
GOE1…GOE6 SOURCE	declared signal name	Routes an ATF pad or macrocell-feedback signal to an internal GOE line.

Target and option	Values	Purpose
GOE1…GOE6 INVERT	ON, OFF	Sets internal GOE polarity. ON is rejected on ATF1502; invert its source equation instead.
output GLOBAL_OE	GOE1…GOE6	Makes an output consume a configured internal GOE source.
registered NODE FAST_INPUT	ordinary INPUT name	Binds a registered NODE directly to an ordinary macrocell input pad. Its equation must be NODE = INPUT.
registered output|NODE XOR	TOGGLE	Selects native toggle-register behavior. The ordinary equation is the active-high toggle condition.

Expression tokens and comments

Token	Meaning	Notes
!A	NOT	Highest precedence.
A & B	AND	Evaluated after NOT.
A ^ B	XOR	Evaluated after AND and before OR.
A | B	OR	Lowest precedence.
(expression)	Grouping	Use parentheses to make evaluation order explicit.
0 and 1	Boolean constants	May be used directly in equations.
// text	Line comment	Continues to the end of the line.
/* text */	Block comment	May span lines. Block comments do not nest.
;	Optional separator	Newlines are whitespace; a semicolon may separate declarations or equations.

Command lookup

Command	Result
rcpld design.rcpld	Compiles the source and writes a same-basename JEDEC after a successful fit.
rcpld --license-status	Shows LIMITED or FULL registration status.
rcpld --install-license /path/to/retrocpld.license	Validates and installs a portable license.
rcpld --license /path/to/retrocpld.license design.rcpld	Uses the specified license for one compilation without installing it.